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2016 Mater. Res. Express 3 066301

(http://iopscience.iop.org/2053-1591/3/6/066301)

Materials Research Express

PAPER

Origin of hole and electron traps in graphene oxide

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RECEIVED
21 January 2016

REVISED
30 May 2016

ACCEPTED FOR PUBLICATION
31 May 2016

PUBLISHED
22 June 2016

Keywords: graphene, graphene oxide, flash memory, traps

Supplementary material for this article is available online

Abstract

Charge-carrier capture/emission processes proceeding with the participation of localized states in graphene oxide (GO) in test structures of $Au/SiO_2/GO/SiO_2/Si$ were examined by charge deep-level transient spectroscopy (Q-DLTS). Two groups of traps capable of capturing both electrons and holes in GO were detected. The energy levels of these groups with reference to the electronic band structure of Si were found to be at $E_V + 0.75$ eV ($E_C - 0.37$ eV) and $E_V + 0.55$ eV ($E_C - 0.55$ eV). Such levels are proposed to be inherent to graphene islands in which charge carriers are emitted from energy levels in the vicinity of the Dirac point. Two groups of levels are suggested to be attributed to graphene islands, with and without p-doping with oxygen.

Introduction

Graphene is a material that exhibits many significant properties such as high electrical and thermal conductivity, very high mobility of charge carriers, high optical transparency and unprecedented mechanical strength [1]. Since the discovery of graphene, a huge number of original studies and reviews devoted to this material has been published. However, today the focus in the field has obviously shifted from studies of graphene itslef to its numerous applications. Graphene enjoys broad prospects for application, from high-mobility graphene-based field-effect transistors (FETs) and transparent conducting materials to photovoltaic and nanophotonic components [2–5]. Among the long list of potential applications of graphene, nonvolatile flash-memory devices deserve special mention [6–12].

Like the total number of on-chip FETs, the total number of on-chip memory cells is continually increasing. However, further miniaturization of the memory cells in flash memory has encountered serious difficulties, which has necessitated the replacement of polysilicon, traditionally used for preparation of floating gates, by some new material. One possible candidate here is graphene. This application of graphene offers advantages over other materials such as a high density of states, a high work function of 4.5–4.6 eV [13, 14], two-dimensionality for increasing gate-coupling ratio and thermal stability. Also, graphene is a mechanically strong yet flexible material, and it therefore offers considerable potential in flexible electronics. The successful application of graphene as a floating-gate material in flash-memory structures has been demonstrated previously [6, 7].

Apart from graphene itself, graphene oxide (GO) can also be used as a floating gate since this material has been shown to be able to trap charges. Moreover, the process for producing GO is quite simple, offering a large yield and low cost of ready material in comparison with graphene [15].

In terms of structure, GO is a highly non-uniform material that involves areas of unmodified graphene and areas of oxidized graphene, the oxidized graphene involving a high density of hydroxyl, carbonyl and epoxy bonds [8]. According to theoretical considerations, oxidized graphene forms a dielectric matrix that may contain embedded graphene inclusions. Such inclusions are thought to be capable of capturing charge carriers. Also, charge carriers can be captured by the chemical bonds in GO. That is why graphene oxide can be considered as a

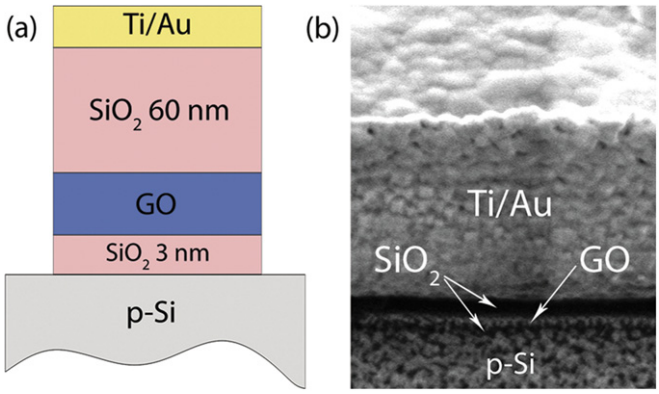

Figure 1. (a) Schematic cross-sectional view of a Au/SiO_2/GO/SiO_2/Si test structure similar to the structure of a nonvolatile flash-memory cell; (b) image of a test structure obtained by scanning electron microscopy at an electron-beam incidence angle 45°.

potentially interesting storage medium for the preparation of floating gates. The successful application of GO and reduced GO as a floating-gate material has been demonstrated in references [9–12]. However, the energy levels of traps for electrons and/or holes in GO have not been investigated yet. Data on those levels, however, are of great significance for understanding capture processes in GO and for the future design of GO-based flash-memory devices. One method that allows the study of electrically active traps in GO and its properties is deep-level transient spectroscopy. Such a technique was used to investigate traps in epitaxial graphene [16].

In the present study, special test structures involving a GO layer were fabricated to examine charge-carrier capture/emission processes proceeding with the participation of the GO layer by means of charge deep-level transient spectroscopy (Q-DLTS). The structure of the samples under study was analogous to the structure of nonvolatile flash-memory cells in which the GO layer served the function of a floating gate. The thickness of control dielectric in our samples was chosen so as to permit tunneling transport of charge carriers between the GO layer and the Si substrate. For the first time, the characteristics of trap levels for electrons and holes in GO and the rates of capture/emission processes in such layers have been evaluated.

Methods

The GO layer was fabricated from a GO suspension obtained by the modified Hammers' method [17]. The obtained GO suspension was then deposited onto a specially prepared Si(100) substrate of p-type conductivity covered by a thin, thermally grown SiO_2 layer of thickness 30 Å. More details of the preparation and deposition of the GO suspension can be found in reference [18] and more details about the GO layer in our structures are given in the supplementary information (see figures S1–S3). Next, the plasma-enhanced chemical vapor deposition (PECVD) process was used to deposit control dielectric SiO_2 of about 60 nm thickness onto the GO layer. After that, evaporation and lift-off photolithography were used to deposit Ti(5 nm)/Au(200 nm) metal gates. To form independent test cells, the layer stack was etched in fluorine-containing plasma (Freon) down to the Si substrate. During the etching, the metal gates acted as a mask. As a result, an array of test structures with lateral dimensions 300 × 300 μm^2 was obtained. The reference samples were prepared as test samples in the same technological cycle, but they did not contain the GO layer.

A schematic cross-sectional view of a prepared test structure is shown in figure 1(a). It illustrates the sequence and the thickness of included layers. Also, a scanning electron microscope image of one of the test structures obtained with the electron beam incident at 45° onto the sample is shown in figure 1(b).

Q-DLTS was used to study the charge-carrier capture/emission processes in the prepared test structures and to determine the characteristics of electron and hole traps in them. The Q-DLTS technique was developed for characterization of the highly resistive or complicated structures with dielectric layers. In the present study, Q-DLTS spectra were measured on an Automatic System of Electrical–Physical Characterization ASEC-03 (see the supplementary materials). In the implemented Q-DLTS procedure, voltage pulses were applied to the metal gate of the measured test structures. Capacitance–voltage characteristics (see figure S4) were used to choose the filling pulse voltage. The peaks observed in the Q-DLTS spectra connected with emission of electrons and holes are usually marked as E and H, respectively.

On applying a negative voltage pulse to the gate the band diagram of the structure changes as shown in figure 2(c). Holes tunnel across the thin SiO_2 layer into GO, where they are captured by traps in GO. After the end of the filling voltage pulse, the system returns to its initial state (figure 2(d)) via activated emission of GO-

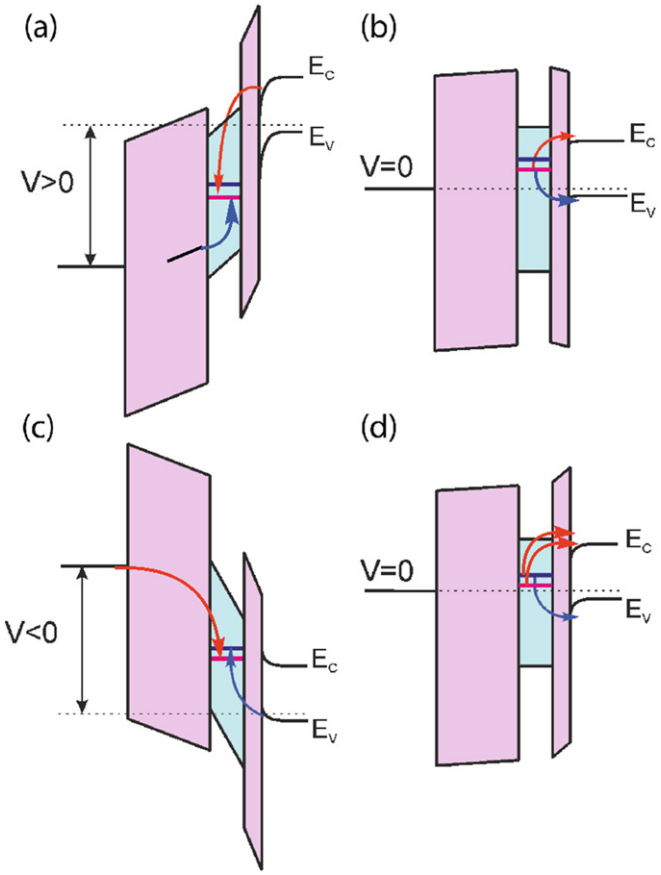

Figure 2. Band diagram of the test structure under a voltage pulse and afterwards: (a) under a positive voltage pulse; (b) after a positive voltage pulse; (c) under a negative voltage pulse, (d) after a negative voltage pulse. The pink color on the band diagrams corresponds to SiO_2 layers, and the blue to the GO layer. The top and bottom edges of the GO energy structure are conditional.

trapped holes with the emergence of a positive peak in the Q-DLTS spectrum. Furthermore, some measurements were performed using a positive voltage pulse. The energy band diagram in this case is as in figure 2(c). Electrons tunnel across the thin SiO_2 layer into GO, where traps capture them. After the end of the filling pulse electrons are emitted from those traps (figure 2(d)). Under such conditions, a positive peak emerging in the Q-DLTS spectrum will be due to electron emission.

Results

The main data obtained in Q-DLTS measurements, namely the Q-DLTS spectra and the Arrhenius plots for the observed peaks, are shown in figure 3. Consider first the data that were obtained on the reference samples (Test-Ref). A representative Q-DLTS spectrum measured on one of the reference samples is shown in the supplementary materials (figure S5). This spectrum involves only one peak H0 due to the capture/emission of holes, and no other peaks in the reference samples were observed for any measurement conditions. However, peak H0 was observed in all measured samples, including the test samples with GO. Arrhenius plots for one of the reference samples (Test-Ref) and for several test samples (Test-GO) are shown in figure S6. The activation energy for the process associated with the H0 peak was found to equal $E_V + 0.30$ eV in the reference samples, where E_V is the top of the Si valence band and $E_V + (0.26–0.34)$ eV in the test samples with the GO layer (see table 1).

In the test samples whose Q-DLTS spectra were measured using negative saturation pulses of a relatively small amplitude (−4 V), an additional negative peak E2 was observed along with the H0 peak. The amplitude of the extra peak, however, was rather small in comparison with that of the H0 peak. The activation energy for the process associated with the E2 peak was found to be $E_C - (0.35–0.38)$ eV for different test structures (figure S7 in the supplementary information; E_C is the bottom of the Si conducting band). We suggest that saturation of the GO traps with electrons could proceed due to electrons tunneling across the control dielectric. Other parameters calculated for the E2 peak are given in table 1.

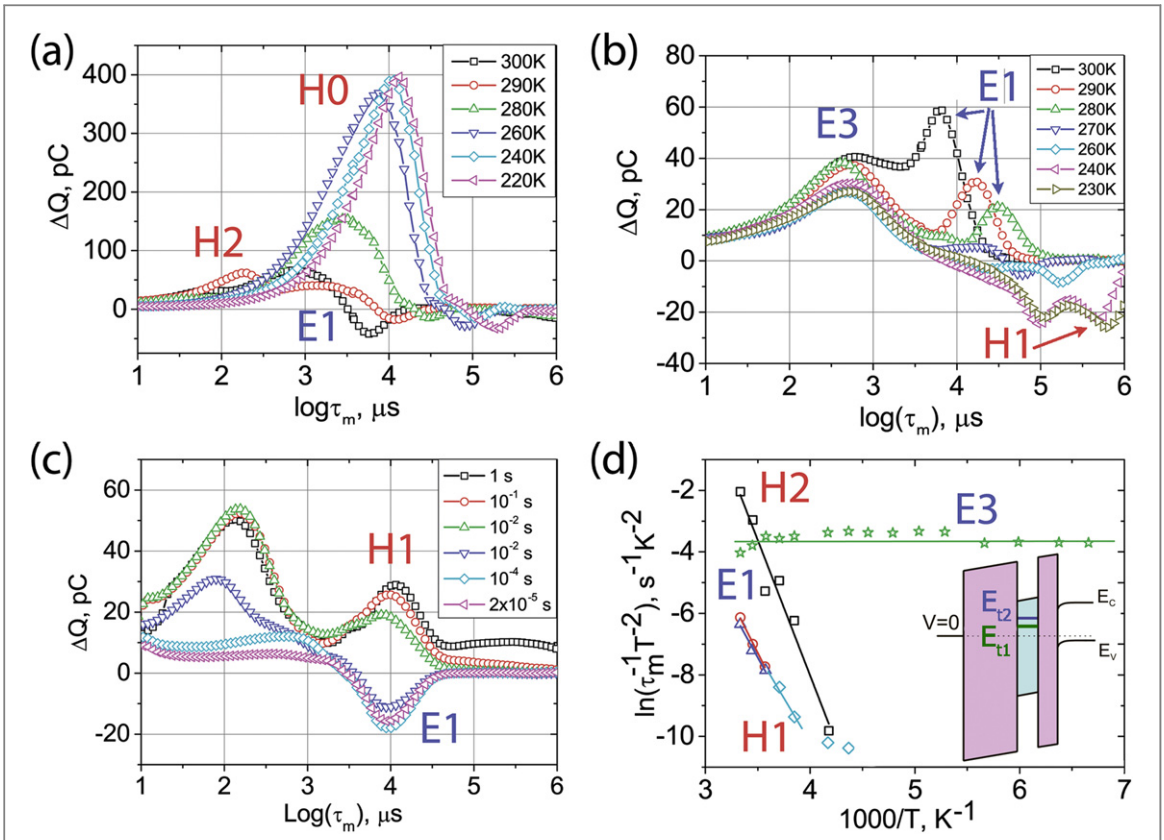

Figure 3. Q-DLTS spectra of a test sample measured at a relatively large (a) negative ($dV = -12$ V) and (b) positive ($dV = 12$ V) amplitude of the filling pulse; (c) Q-DLTS spectra measured for various duration of filling pulse (given as a parameter) at room temperature; (d) several Arrhenius plots for peaks H1, H2, E1 and E3 measured at $dV = \pm 12$ V. The inset shows the schematic band diagram of a test structure with trap levels $E_{t1} = E_C - 0.55$ eV and $E_{t2} = E_V + 0.75$ eV without an applied voltage. Pink color corresponds to SiO_2 layers and blue to the GO layer.

Table 1. Characteristics of traps observed by Q-DLTS: E_a is the activation energy; N_t is the trap concentration; ΔT is the temperature range for trap observation and characteristic times for charge-carrier emission at room temperature τ_m.

Filling pulse	Traps	E_a (eV)	N_t (10^{12} cm^{-2})	ΔT (K)	τ_m (μs) (at $T = 300$ K)
			Test-Ref		
−4 V −12 V +12 V	H0 H3	0.30 0.00–0.05	0.7–2.7 0.3	300−80 80–220	2×10^3 4.8×10^3
			Test-GO		
−4 V	H0	0.26–0.34	2.6–4.7	220–300	$(1–1.8) \times 10^3$
	E2	0.35–0.38	0.5–4.7	230–300	$(1.8–15) \times 10^3$
	H3, E3	0.00–0.05	0.3–0.8	80–230	$(4–5) \times 10^3$
−12 V	H0	0.26–0.29	8.6	260–300	600
	H2	0.75	2.7	240–300	100
	E1	0.55	0.8	280–300	$(4.4–5.7) \times 10^3$
	E3, H3	0.00–0.05	0.3–0.8	80–240	$(4–5) \times 10^3$
+12 V	E1	0.55	1–1.6	280–300	6.6×10^3
	H1	0.55	—	250–270	—
	H3, E3	0.00–0.05	0.3–0.8	80–230	$(4–5) \times 10^3$

An increase in filling pulse magnitude to −12 V leads to the emergence of additional peaks in the Q-DLTS spectra shown in figure 3(a). Two peaks, H2 and E1, are distinctly observed in the spectra. The Arrhenius plots for these peaks are shown in figure 3(d). The activation energies for the H2 and E1 processes are $E_V + 0.75$ eV and $E_C - 0.55$ eV, respectively (see table 1).

Q-DLTS spectra measured on GO samples biased with a positive voltage pulse of amplitude +12 V are shown in figure 3(b). Evidently, on changing the saturation pulse to the opposite polarity, the Q-DLTS spectra have changed dramatically. Three peaks—E1, E3 and H1—were observed in the spectra. The position of the E3 peak remains unchanged with varying temperature, thus proving that the electron emission here was a nonactivated process. The E1 peak was observed at temperatures 300–280 K and disappeared at lower temperatures, whereas the H1 peak appeared only at lower temperatures, starting from 270 K. Arrhenius plots for the Q-DLTS peaks E1, H1 and E3 are shown in figure 3(b). The activation energy for the E1 process was found to be $E_C - 0.55$ eV. However, the experimental points for the H1 peak are clearly seen to fit a single straight line passing through the experimental points for the E1 peak (figure 3(d)). Therefore, we suggest that processes E1 and H1 have the same value of activation energy but counted from different (conducting and valence) bands of Si (table 1).

A similar sign-alternating pattern of Q-DLTS peaks was observed when varying the charging time at constant temperature. Q-DLTS spectra measured at different charging times are shown in figure 3(c). With decreasing charging time, the H1 peak was substituted by the E1 peak in the spectra. This phenomenon may be due to different concentrations of the two traps and to different values of the characteristic times for capture/emission of different charge carriers (electrons and holes) by/from the traps of the two types. We would like to mention here that, in the reference samples, no peaks due to electron traps were observed on variation of the duration of the saturation pulse.

Discussion

Now let us discuss the most important traps in GO connected with peaks H1, E1, H2 and E2 that were observed in the test samples. First of all let us consider the conditions to observe both electron and hole traps as examples of E1 and H1 peaks. These peaks appear when a positive voltage pulse is applied. The band diagram of the structure for this case is shown in figure 2(a, b). The electrical field during the filling pulse is provided by tunneling of electrons from the substrate through the thin (30 Å) SiO_2 layer into GO. Emission of these electrons results in the appearance of the E1 peak. However, the H1 peak connected with holes is also observed in the same conditions. Holes cannot come from both Si substrates and the metal gate. However, the control dielectric SiO_2 contains many defects and traps, including hole traps able to generate holes in a high electrical field. We suggest that these holes captured by the traps in the GO layer are responsible for the H1 peak.

The sum of the activation energies for the emission of electrons and holes is approximately equal to the bandgap energy of Si. Indeed, with reference to table 1, we have $E1 + H1 = 0.55 + 0.55 = 1.1$ eV. In the Arrhenius plots, the E1 peak was substituted for the H1 peak at some temperatures (see figure 3(b)) or at different charging times (see figure 3(c)). So, the E1 peak disappears from the spectra when the H1 peak appears in them. Most likely, these two peaks are caused by two parallel processes competing with each other. Such behavior can be attributed to a situation in which two states with close energy levels are involved in emission processes for electrons and holes. Such behavior may be due to the emission of charge carriers from energy levels near the Dirac point in graphene (above and below). Since GO is thought to be structurally non-uniform and to contain areas of unmodified graphene, we consider that in test structures such areas are involved in the capture and emission of charge carriers, resulting in the appearance of E1 and H1 peaks.

A further argument that E1 and H1 peaks are connected to graphene islands is matching of the graphene work function and the difference between electron vacuum energy and trap level. The graphene work function is equal to 4.5–4.6 eV [13, 14] and the silicon work function to 4.05 eV. Indeed, the sum of trap energy $E_C - 0.55$ eV and the silicon work function is approximately equal to the graphene work function. So, E1 and H1 peaks correspond to undoped graphene islands.

E2 and H2 peaks appeared when a negative voltage pulse was applied. In this case, the band diagram of the structure is shown in figure 2(c, d). In this electrical field holes tunnel from the substrate through the thin SiO_2 layer into GO during the filling pulse. Hole emission after the end of the filling pulse results in the appearance of the H2 peak. The E2 peak is connected with electrons that come from the metal gate through the control dielectric SiO_2. The sum of the activation energies for E2 and H2 peaks is again equal to the bandgap of Si $E2 + H2 = 0.37 + 0.75 = 1.12$ eV. Following the explanation given above for E1 and H1 peaks, we suggest that E2 and H2 peaks correspond to graphene islands with p-type doping. Doping is most likely provided by oxygen.

Let consider the traps H0 observed in all our structures including the reference ones. In the reference samples these traps have an activation energy of $E_V + 0.30$ eV (see figure S5 in the supplementary information). It is well known that defects called P_b centers are generally observed at the Si–SiO_2 interface. P_b centers have been identified as the dangling bonds of Si atoms and they introduce a level located at an energy $E_V + 0.30$ eV [19]. Evidently, the traps H0 observed in the reference samples are connected with the P_b centers at the Si–SiO_2 interfaces. Similar traps observed in all examined test samples (figure S6) are also suggested to correspond to P_b

centers. However, in the latter case the activation energy varied in the interval from $E_V + 0.24$ to $E_V + 0.34$ eV (see table 1). The different values of activation energy are probably due to the influence of GO on the P_b centers or on their surroundings, resulting in enhanced potential fluctuations at the Si–SiO_2 interfaces.

In almost all measured test samples, traps with very small or even zero values of activation energy were observed (peaks E3 and H3). Such peaks emerged in the Q-DLTS spectra at relatively low temperatures (below 250–230 K) due to the escape of charge carriers from GO traps via their tunneling emission across the thin (30 Å thick) SiO_2 layer into Si or via tunnel hops over traps in the control dielectric SiO_2 into the gate. These traps are not of interest from the viewpoint of the present study of GO-related traps and their potential application in GO-based flash-memory devices.

Conclusion

In conclusion, the test structures of Au/SiO_2/GO/SiO_2/Si involving GO layers have been examined by means of Q-DLTS. The main traps found in the test structures with GO layers were two groups of traps whose levels were located roughly level with the mid-gap energy of Si, at approximately $E_V + 0.55$ eV and $E_V + 0.75$ eV. Emission of both types of carriers from those levels—holes into the valence band of Si and electrons into its conduction band—was observed. Presumably, the detected traps correspond to graphene islands of either neutral conductivity or p-type conductivity resulting from the doping with oxygen.

Acknowledgments

This study was supported in part by the Russian Foundation for Basic Research under Grant No. 15-02-02189.

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